AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claim 1 (Currently Amended): A semiconductor device having a multilayer wiring structure, comprising:

a semiconductor substrate;

a lower ~~wiring~~ dielectric layer arranged on the substrate and having an opening, a conductive portion filling the opening, and at least one dielectric member embedded in the conductive portion;

an interlayer dielectric film arranged on the lower ~~wiring~~ dielectric layer and having a contact wiring; and

an upper ~~wiring~~ dielectric layer arranged on the interlayer dielectric film and having an upper opening, an upper conductive portion filling the upper opening, and at least one dielectric member embedded in the upper conductive portion, wherein the upper ~~wiring~~ dielectric layer and the lower ~~wiring~~ dielectric layer are electrically connected by the contact wiring.

Claim 2 (Original): The semiconductor device according to claim 1, wherein at least one dielectric member is arranged in an island-like manner in the opening.

Claim 3 (Canceled).

Claim 4 (Original): The semiconductor device according to claim 1, wherein the conductive portion includes an external electrode terminal.

Claim 5 (Withdrawn): A method for manufacturing a semiconductor device comprising:

forming an opening in a dielectric film arranged above the semiconductor substrate so as to leave a dielectric projection in the opening;

filling the opening with a metal; and

flattening the surface of the metal using the upper surface of the dielectric film as a stopper.

Claim 6 (Currently Amended): A semiconductor device having a multilayer wiring structure, comprising:

a semiconductor substrate;

a lower [wiring] dielectric layer arranged on the substrate and including an upper surface, a lower surface, an opening, at least one dielectric member arranged in the opening, and a conductive portion filling the opening so as to surround the at least one dielectric member;

an interlayer dielectric film arranged on the lower [wiring] dielectric layer and having a contact wiring; and

an upper [wiring] dielectric layer arranged on the interlayer dielectric film and having an upper opening, at least one dielectric member arranged in the upper

opening, and a conductive portion filling the upper opening so as to surround the at least one dielectric member, wherein the upper [wiring] dielectric layer and the lower [wiring] dielectric layer are electrically connected by the contact wiring.

Claim 7 (Original): The semiconductor device according to claim 6, wherein the dielectric member has a height that is the same as the thickness of the dielectric film.

Claim 8 (Original): The semiconductor device according to claim 6, wherein the dielectric member has an end flush with the upper surface of the dielectric film and a further end flush with the lower surface of the dielectric film.

Claim 9 (Original): The semiconductor device according to claim 6, wherein the at least one dielectric member is one of a plurality of separated dielectric members.

Claim 10 (Original): The semiconductor device according to claim 6, wherein the conductive portion has a flat surface flush with the upper surface of the dielectric film.

Claim 11 (Withdrawn): A method for manufacturing a semiconductor device comprising:

forming a dielectric film arranged above a semiconductor substrate;

forming an opening in the dielectric film so as to leave a dielectric projection in the opening by removing part of the dielectric film;

filling the opening with a metal; and

flattening the metal so the upper surface of the dielectric film is flush with the upper surface of the metal.

Claim 12 (Currently Amended): A semiconductor device comprising:

a semiconductor substrate;

a lower [wiring] dielectric layer arranged on the semiconductor substrate and having a lower pad, wherein the lower pad includes a lower through hole, a lower conductive metal filling the lower through hole, and at least one dielectric member enclosed by the conductive metal;

an interlayer dielectric film arranged on the lower [wiring] dielectric layer and having a contact wiring; and

an upper [wiring] dielectric layer arranged on the interlayer dielectric film having an upper pad, wherein the upper pad includes an upper through hole, an upper conductive metal filling the upper through hole, and at least one dielectric member enclosed by the conductive metal, and wherein the upper conductive metal is electrically connected to the lower conductive metal via the contact wiring of the interlayer dielectric film.

Claim 13 (Previously Presented): The semiconductor device according to claim 12, wherein the lower conductive portion and the upper conductive portion are arranged vertically.

Claim 14 (Previously Presented): The semiconductor device according to claim 13, wherein the contact wiring of the interlayer dielectric film includes a through hole, a conductive metal filling the through hole, and at least one dielectric member enclosed by the conductive metal.